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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/597,523 | 06/20/2000 | Harry J. Beatty III | FIS9-1999-0317-US1 | 5256 |

29505 7590 03/11/2004

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| EXAMINER | |
|---|---|
| PATEL, ASHOKKUMAR B | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2154 | |

DATE MAILED: 03/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/597,523 | BEATTY III ET AL. | |
| | Examiner | Art Unit | |
| | Ashok B. Patel | 2154 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *1/29/2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-4,6-11,13,15 and 17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-11,13,15 and 17* is/are rejected.

7)☒ Claim(s) *5,12,14,16,and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1-18 are subject to examination.

### *Response to Arguments*

2. Applicant's arguments filed January 29, 2004 have been fully considered but they are not persuasive for the following reasons:

### *Claim Rejections - 35 USC § 103*

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

**Referring to claims 1-4, 6-8, 9 and 10,**

4. Claims 1-4, 6-8, 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Meyer (6,397,299) in view of CAI et al. (hereinafter CAI) (Pub. No. US 2001/0049770 A1.).

In response to applicant's arguments, the recitation Parallel computing has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951). Also, in response to applicant's arguments against the references individually, one cannot

show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). The reference Meyer teaches that the memory can be configured as a subset of the main memory. (Abstract). Thereby, it teaches that the subset of the memory (a level of hierarchy) can be created and configured as a memory structure. This teaching is considered a significant concept for any type of computing environment, although it does not specifically teach parallel computing. As such, this reference is considered analogues. The reference CAI teaches, as indicated before, CAI teaches, "**A buffer memory in the system has multiple buffer sections.** Each buffer section is **adapted to store information associated with requests from a corresponding one of the multiple execution entities**., page 1, paragraph [0008]. " For example, a **program execution entity**, such as a process, task, or **thread**, associated with a multimedia application may transfer large blocks of data (e.g., video data) that are typically not reused., page 1, paragraph [0005]. Each buffer section may be **a separate buffer module** or may be **a portion of a buffer memory that is separately addressable** (that is, memory is separated into different address spaces)., page 1, paragraph [0017]." CAI also teaches, "The individual buffer sections may be **separately configurable** and may be assigned to store information of **different program execution entities in the system**.", page 1, paragraph [0017]. The reference teaches the multi-unit buffer memory configuration in a computing environment such as multithreading allowing parallelism. Also, the reference teaches that the each buffer is configurable (containing

the same or different program structures) as a portion of a buffer memory where each buffer section is adapted to store information associated with requests from a corresponding one of the multiple execution entities such as a thread and which is separately addressable (independent flow of control).

The reference Kinoshita et al. (US 4, 703, 422, is included herein teaching a memory hierarchy control method for a memory hierarchy system having a plurality of hierarchy levels. (Col. 1, lines 52-55) and clearly teaches having two or more hierarchy storages of different access speeds and programs. (Abstract).

**Referring to claims 11, 13, 15 and 17**

Keeping in mind the response as stated above for the claims 1-4, 6-8, 9 and 10, the EID that CAI teaches is an identifier assigned to the execution entity that is a thread. [0021. And as stated in the previous office action, independent modules of multi-unit memory is assigned to store information of corresponding execution entities. Therefore, the reference teaches that each module can have its own execution entity, which can be a thread as taught by CAI.

**Referring to claims 5, 12, 14, 16 and 18,**

Claims 5, 12, 14, 16 and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ashok B. Patel whose telephone number is (703) 305-2655. The examiner can normally be reached on 8:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John A Follansbee can be reached on (703) 305-8498. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Abp
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JOHN FOLLANSBEE
SUPERVISORY PATENT EXAMINER
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